Remarks

Receipt is acknowledged of the Office Action mailed November 2, 2004. Claims 1-10 and 19-20 were pending in the application. Claims 11-18 were withdrawn from further consideration as being drawn to a nonelected group of claims. Claims 11-18 have been canceled without prejudice or disclaimer. Claims 1-3, 19 and 20 have been amended. No new matter has been introduced. Thus claims 1-10 and 19-20 are pending for reconsideration at this time.

Applicant thanks the Examiner for acknowledging receipt of the priority documentation in the pending application and for the continuing examination of the pending application.

Applicant also thanks the Examiner for acknowledging receipt of the Information Disclosure Statement filed on July 25, 2003.

Allowable Subject Matter

Applicant acknowledges with appreciation the indication of allowable subject matter in claims 3-8.

The Office Action states that claims 3-8 must be rewritten to overcome the rejections under 35 U.S.C. §112, ¶2 as set forth in this Office Action. However, no rejection under 35 U.S.C. §112, ¶2 is set forth in the Office Action. Hence, Applicant assumes this statement refers to the rejection under 35 U.S.C. §112, ¶1 as stated on page 2 of the pending Office Action. The rejection of claims 3-8 under 35 U.S.C. §112, ¶1 is addressed below.

Claims 3-8 are dependent upon claim 1, and are believed to be allowable for at least the following reasons with respect to claim 1, in addition to the further patentable features recited therein. Allowance of claims 3-8 is solicited.

Rejections Under 35 U.S.C. §112, ¶1

Claims 1-10 stand rejected under 35 U.S.C. §112, ¶1 as failing to comply with the written description requirement. Claims 1-10 allegedly contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Specifically, the Office Action acknowledges that FIG. 7 shows a register controller 510 comprising a register array 511 and a register command processor 512. The Office Action asserts, however, that there is no drawing showing a register controller comprising a nonvolatile memory unit, a register array, and a register command processor as claimed in claim 2. Applicant respectfully traverses this rejection for at least the following reasons.

In regards to claims 1, 9 and 10, the Office Action fails to specify any deficiency though these claims are rejected under 35 U.S.C. §112, ¶1. The Office Action specifies a deficiency regarding the register controller "as claimed in claim 2" which is relevant to claim 2, and also to claims 3-8 based on their dependency upon claim 2. None of claims 1, 9 or 10, however, are dependent upon claim 2. As no deficiency has been specified in reference to claims 1, 9 and 10, withdrawal of the rejection of claims 1, 9 and 10 under 35 U.S.C. §112, ¶1 is solicited.

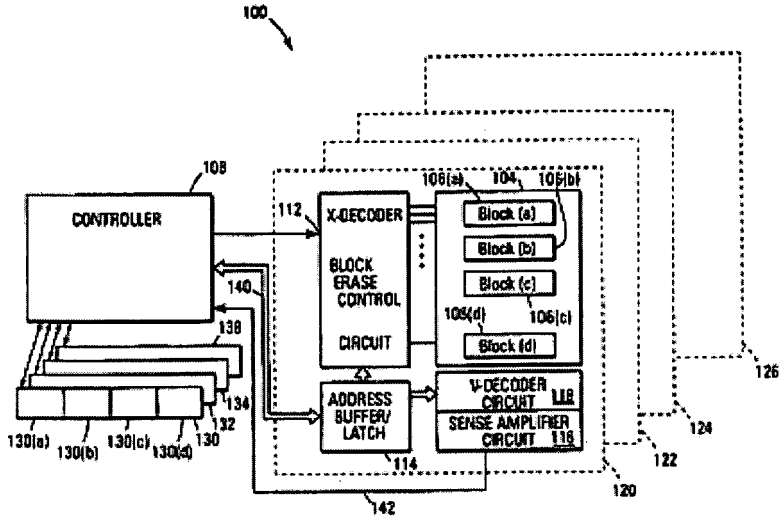
In regards to claims 2-8, Applicant directs the Examiner's attention to FIG 16, which shows a register included in a memory device. This register includes nonvolatile ferroelectric capacitor(s) that function as a nonvolatile memory unit as claimed (see pg. 20, line 1 to pg. 22, line 6 of the as-filed specification). Given this disclosure, Applicant clearly had possession of the claimed invention at the time the application was filed. Withdrawal of the rejection of claims 2-8 under 35 U.S.C. §112, ¶1 is solicited.

Rejections Under 35 U.S.C. §102

Claims 1, 2 and 19 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,614,695 ("Keays" hereafter). Claim 19 also stands rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,484,278 ("Merritt" hereafter). Applicant respectfully traverses these rejections for at least the following reasons.

U.S. Patent No. 6,614,695 (Keays)

As shown in FIG. 1, Keays discloses a mass storage flash memory 100 including a flash memory 120 (col. 4, lines 60-61). FIG. 1 is reproduced below for the Examiner's convenience.



Claims 1 and 2

The Office Action asserts Keays discloses a non volatile memory unit 104, and a register controller 108, 130. Keays discloses a flash memory 120 with an array 104 of non-volatile memory cells (col. 4, lines 61-62), and a controller 108 for controlling memory operations (col. 5, lines 14-18). In reference to element 130, Keays discloses a register 130 associated with flash memory array 104 on flash memory 120. The disclose structure in Keays does not, however, correspond to the claimed register controller, because it does not store control data used to control a parameter controller as claimed.

The controller 108 of Keays controls ordinary flash memory functions such as "program", "erase" and "read" (col. 5, lines 15-18). In cooperation with the controller 108 and flash memory 120, the register 130 stores flags indicating whether data has been erased (col. 5, line 58-col. 6, line 5). However, there is no disclosure in Keays of the controller 108 causing the register 130 or flash memory array 104 to store control data used to control a parameter controller as claimed.

Moreover, the flash memory array 104 of Keays is simply a data storage array, forming part of the mass storage flash memory 100 (col. 4, lines 56-58). There is no disclosure in Keays of the flash memory array 104 being used to store *control* data as claimed. As Keays fails to disclose or suggest a structure that stores control data used to control a parameter controller as presently claimed, it fails to anticipate the presently claimed invention.

In addition, the Office Action asserts that Keays discloses a parameter controller 112,

114, 116 configured to output a signal having a characteristic parameter depending on a signal outputted from the register controller 108, 130. Elements 112, 114, 116 correspond to an x-decoder/block erase control circuit 112 (col. 5, line 6), an address buffer/latch 114 (col. 5, line 5), and a sense amplifier circuit 116 (col. 5, lines 21-22) respectively. The disclosed structure in Keays, however, does not correspond to the claimed parameter controller, because it does not output a signal having a characteristic parameter depending on control data outputted from the register controller as claimed.

The controller 108 in Keays is coupled to the address buffer/latch 114 by address line 140 *to provide address requests* (col. 5, lines 18-21). The address buffer/latch 114 is further coupled to the x-decoder circuit/block erase control 112 and the y-decoder circuit 118 to provide the address requests to these circuits 112, 118 (col. 5, line 4-7). There is no disclosure in Keays, however, to indicate the output of address buffer/latch 114 has a characteristic parameter depending on control data outputted from the controller 108. Rather, the address buffer/latch 114 simply receives, latches, and outputs the address requests from controller 108.

The controller 108 is further coupled to the x decoder/block erase control circuit 112 *to control erase operations on the memory array 104* (col. 5, lines 23-26) and to the sense amplifier circuit 116 via data line 142 *to provide the controller with the results of a cell that is read or verified* (col. 5, lines 21-23). Essentially, the sense amplifier circuit 116 verifies the erasure of blocks of memory and provides the results to the controller 108, which in turn stores the results in register 130 (col. 5, lines 58-62). There is no disclosure in Keays, however, to indicate the signal outputted by sense amplifier circuit 116 has a characteristic parameter depending on control data outputted from the controller 108.

As the structure corresponding to elements 112, 114, 116 in Keays does not output a signal having a characteristic parameter depending on control data outputted from controller 108 as claimed, it cannot anticipate the presently claimed invention for this additional reason. Withdrawal of the rejection under 35 U.S.C. §102(e) of claims 1 and 2 over Keays is solicited.

Independent Claim 19

The Office Action states on page 3 that claim 19 "is rejected under 35 U.S.C. 102(e)

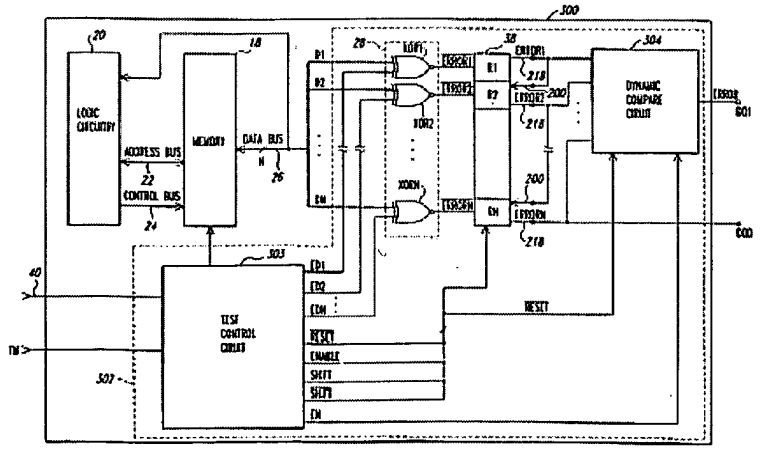
[over Keays] since it recited similar limitations as in claim 1." The rejection of claim 19 is thus traversed for similar reasons as stated above with respect to claim 1, and discussed in greater detail below.

Claim 19 recites a signal performance characteristics controller that controls the signal performance characteristics of the input signal and makes it outputted at the integrated circuit device as an output signal. The claimed signal performance characteristics corresponds to the register controller and parameter controller recited of claim 1. These elements, the register controller and the parameter controller, are not disclosed by Keays as discussed above with respect to claim 1. As such, Keays fails to anticipate claim 19 for similar reasons as stated above with respect to claim 1. Withdrawal of the rejection of claim 19 under 35 U.S.C. §102(e) over Keays is solicited.

U.S. Patent No. 6,484,278 (Merritt)

The Office Action asserts that Merritt discloses in FIG. 4 an integrated circuit device capable of receiving an input signal and generating an output signal having signal performance characteristics comprising a signal performance characteristic controller (302) configured to control one or more of the signal performance characteristics (DQ) of the integrated circuit device. Applicant respectfully disagrees.

FIG. 4 in Merritt is a functional block diagram of an Embedded DRAM 300 including a test circuit 302 (col. 8, lines 28-30), a memory 18, and logic circuitry 20 (see FIG. 4). FIG. 4 is reproduced below for the Examiner's convenience.



The test circuit 302 of Merritt activates an error signal on DQ1 to identify defective addressed memory cells (col. 8, lines 63-66; col. 9, lines 63-65). This error signal does not have a *performance characteristic* controlled by the test circuit 302 as claimed. Rather, it is merely used to control testing of a read operation of the memory.

In contrast, the signal performance characteristic controller controls the signal performance characteristic of an output signal. As no such structure is disclosed or suggested by Merritt, it fails to anticipate claim 19. Withdrawal of the rejection under 35 U.S.C. §102(e) over Merritt is solicited.

Rejections Under 35 U.S.C. §103(a)

Claims 9 and 10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Keays and U.S. Published Application No. 2004/0047172 ("Komatsuzaki" hereafter). Claims 9 and 10 are dependent upon claim 1, and are allowable for at least the aforementioned reasons with respect to claim 1 in addition to the further patentable features recited therein.

Claim 20 stands rejected under 35 U.S.C. §103(a) over Merritt. Claim 20 is dependent upon claim 19, and is allowable for at least the aforementioned reasons with respect to claim 1 in addition to the further patentable features recited therein.

Allowance of claims 9, 10 and 20 is solicited.

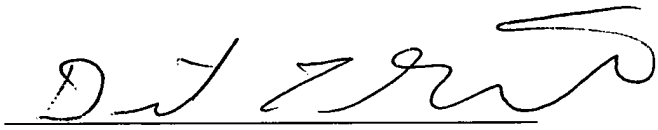
Conclusion

In view of the above amendments and remarks, Applicant respectfully requests that all objections and rejections be withdrawn and that a notice of allowance be forthcoming. The Examiner is invited to contact the undersigned for any reason related to the advancement of this case.

The Commissioner is authorized to credit any over payment or charge any deficient to deposit account number 08-1641.

Respectfully submitted,

Date: February 1, 2005

By: 

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